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A 2D Heterostructure-Based Multifunctional Floating Gate Memory Device for Multimodal Reservoir Computing

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The demand for economical and efficient data processing has led to a surge of interest in neuromorphic computing based on emerging two-dimensional (2D) materials in recent years. As a rising van der Waals (vdW) *p*-type Weyl semiconductor with many intriguing properties, tellurium (Te) has been widely used in advanced electronics/optoelectronics. However, its application in floating gate (FG) memory devices for information processing has never been explored. Herein, an electronic/optoelectronic FG memory device enabled by Te-based 2D vdW heterostructure for multimodal reservoir computing (RC) is reported. When subjected to intense electrical/optical stimuli, the device exhibits impressive nonvolatile electronic memory behaviors including ≈10^8 extinction ratio, ≈100 ns switching speed, >4000 cycles, >4000-s retention stability, and nonvolatile multibit optoelectronic programmable characteristics. When the input stimuli weaken, the nonvolatile memory degrades into volatile memory. Leveraging these rich nonlinear dynamics, a multimodal RC system with high recognition accuracy of 90.77% for event-type multimodal handwritten digit-recognition is demonstrated.

1. Introduction

Ultrathin two-dimensional (2D) materials, featured with atomically thin thickness and dangling-bond-free layered surface can be easily integrated into a wide range of van der Waals (vdW) heterostructures for advanced electronics/optoelectronics with desired functionalities, thus shedding light on extending Moore's law and breaking the von Neumann bottleneck in the era of big data.[1–3] Reservoir computing (RC) based on 2D materials highlighting low training complexity and high energy efficiency offers a promising solution to the ever-increasing data volume.[4–9] Researchers have leveraged the ferroelectricity in 2D α-phase indium selenide (α-In_2Se_3) to construct a stackable RC system for hierarchical information processing,[6] and also realized a RC system for image recognition with

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low-energy consumption using the charge-trap memory in the 2D molybdenum disulfide (MoS_2) channel.[7] Moreover, an in-sensor RC system for language learning has been reported based on the photoelectricity in 2D tin sulfide (SnS).[8] However, the data generated by smart devices in our daily lives is typically multimodal, posing a huge challenge to existing RC systems that are dedicated to single modality learning. Promisingly, Liu et al. reported a multimodal RC system based on 2D α-In_2Se_3 for multimodal handwritten digit recognition recently.[9] However, in their simulation, the input signals are limited to nonevent signals, and their device cannot serve as long-term memory unit.

The construction of 2D RC systems has largely relied on devices in the diode geometry, while emerging three-terminal transistor-geometry memory devices show potential as an ideal data processing platform due to their versatile control parameters and high compatibility with traditional complementary metal-oxide-semiconductor (CMOS) devices.[10–12] Although 2D material-based three-terminal memory devices include ferroelectric field-effect transistors (FeFETs) and floating gate (FG) memory devices, the latter typically presents greater application prospects with its ultrafast operation speed,[10,11] facile extension in the vertical dimension,[13] and the achievement of logic-in-memory in 2D FG transistor-based computing systems.[14,15] While electrical control is the most common method to operate 2D FG devices, optical sensitivity is indispensable for realizing multimodal (RC). The choice of the FG material is therefore vital to endow 2D FG memory units with both electrical and optical operations. Although optoelectronic memory has been reported among heterostructures with graphene, 2D perovskites, and MoS_2 nanoflakes as the FG layers, their best-known feature is the nonvolatile optoelectronic memory, rather than the nonlinear fading behavior after switching off the optical pulse.[16–19] Tellurium (Te) is a recently rediscovered vdW semiconductor that features a one-dimensional (1D) crystal structure and presents many interesting properties, including thickness-dependent bandgap, thermoelectricity, and piezoelectricity.[20,21] It has been used to construct various advanced electronics and optoelectronics, such as *p*-type field-effect transistors (FETs) with high room-temperature hole mobility, short-wave infrared photodetectors, three-dimensional (3D) monolithic circuits, and memory units in in-sensor RC at the optical communication band.[22–26] Moreover, as a Weyl semiconductor, the peculiar band structure and spin properties originating from its composition of parallel 1D spiral molecular chains enable its applications in building low energy-consumption valley transistors.[27,28] Moreover, Te demonstrates exceptional potential as a FG material for developing 2D FG memory units due to its distinct band splitting[29,30] and rapid charge recombination at shallow trap states.[31] This material combining with MoS_2 channel offers an added advantage of exhibiting nonlinear electronic/optoelectronic memory which occurs following the attenuation of stimulus intensity.

In this work, we first present a MoS_2/hexagonal boron nitride (h-BN)/Te heterostructure on silicon dioxide/silicon (SiO_2/Si) substrate, where MoS_2 serves as the semiconducting channel, h-BN functions as the tunnel dielectric, Te functions as the FG, and SiO_2 and heavily doped Si are used as a gate oxide and a control gate, respectively. We report on the nonvolatile/volatile electrically and optically controlled memory behaviors of this device by carefully tunning the stimulus intensity. Under intense electrical pulse stimulation, the fabricated device exhibits superior nonvolatile electronic memory performance including fast switching speed (≈100 ns), a high extinction ratio (≈10^8), long cycle (>4000 cycles), and retention (>4000 s) stability, which are comparable to the most advanced 2D FG memory devices. Similarly, under intense optical pulse illumination, this device presents multibit nonvolatile optoelectronic memory behavior. More interestingly, when the stimulus intensity is weakened, we observe nonlinear fading memory behavior attributed to the charge trapping states in MoS_2. Based on these rich, dynamic memory behaviors, we design a RC system for multimodal signal processing, which achieves a high accuracy of 90.77% on the event-based handwritten digit dataset, even surpassing the nonevent digits classification using 2D material-based RC. Our demonstration of this multifunctional 2D FG device will enrich the field of 2D electronics/optoelectronics and thus pave the way for future smart computing systems at the edge.

2. Results and Discussion

2.1. Fabrication and Characterization of the Mos_2/h-BN/Te Heterostructure

In this paper, we present a 2D vdW heterostructure-based electronic/optoelectronic FG memory device, which consists of Te as the FG, h-BN as the tunnel dielectric, multilayer MoS_2 as the channel, and SiO_2/heavily doped Si (p++ Si) as the gate oxide/control gate, respectively, as illustrated in **Figure 1a**. The source/drain electrodes were defined by using standard electron beam lithography (EBL) and thermal evaporation of chromium/gold (Cr/Au) (8/60 nm). The false-color scanning electron microscope (SEM) image in Figure 1b shows the general layout of the MoS_2/h-BN/Te heterostructure on the SiO_2/p++ Si (SiO_2: 50 nm) substrate. The thickness of each material (MoS_2: ≈4.35 nm; h-BN: ≈12.81 nm; Te: ≈27.37 nm) was characterized using atomic force microscope (AFM), as shown in Figure S1 (see the Supporting Information). The heterostructure was stacked from the drop-casting solution-synthesized Te nanoflakes onto the SiO_2/Si substrate,[23] followed by transferring freshly exfoliated h-BN and MoS_2 nanoflakes step by step via a dry transfer method.[32] Details on material preparation and heterostructure fabrication can be found in the Experimental Section and Figure S2 (Supporting Information). Raman spectra were used to identify the involved vdW nanoflakes, as shown in Figure 1c. The Raman spectrum of Te revealed three peaks (E_1: 93.3 cm^{-1}, A_1: 120.6 cm^{-1}, E_2: 142.0 cm^{-1}), which are consistent with previous literature. Additionally, the lattice vibration mode (E_{2g}: 1367.4 cm^{-1}) in h-BN nanoflakes further supports these findings.[22,23,33] The frequency difference of 24.5 cm^{-1} between the E^1_{2g} (383.3 cm^{-1}) and A_{1g} (407.8 cm^{-1}) modes in the Raman spectrum indicates the multilayer nature of MoS_2.[34] Furthermore, the Raman spectrum measured on the final MoS_2/h-BN/Te heterostructure confirms its constitution. To confirm the device structure and demonstrate the clean and flat interfaces between the vdW materials, the cross-section transmission electron microscopy (TEM) was conducted. The left panel in Figure 1d shows the scanning transmission electron microscopy (STEM) on the cross-section cut from the fabricated heterostructure via

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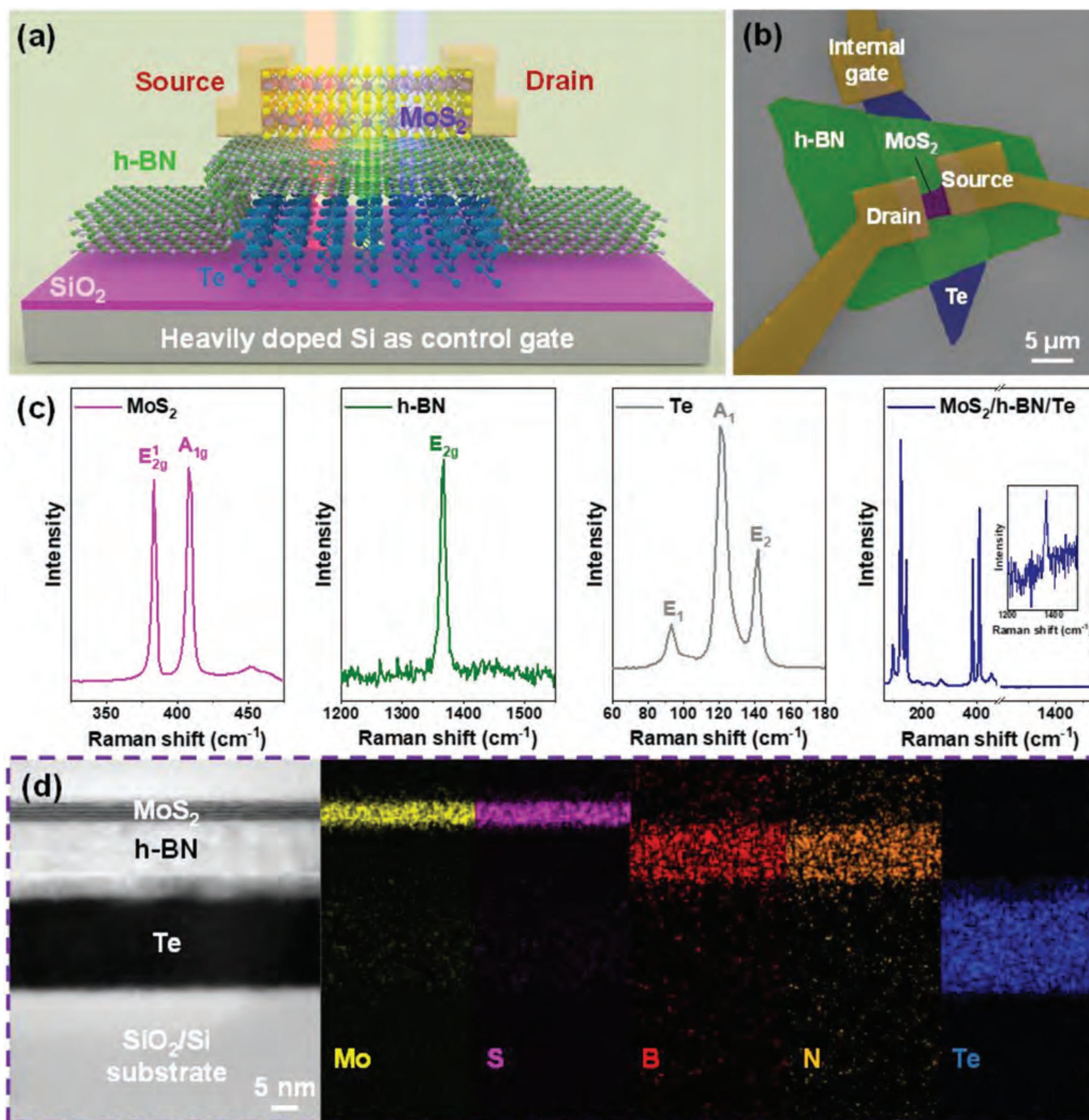

Figure 1. Heterostructure characterization. a) Schematic illustration of the FG memory device based on MoS_2/h-BN/Te heterostructure. b) False-color image of a typical device illustrates the general layout of the device. Different materials and electrodes are marked in different colors. c) Raman spectra of the involved materials in MoS_2/h-BN/Te heterostructure. d) Cross-sectional STEM image and the corresponding EDS mapping of MoS_2/h-BN/Te heterostructure.

focused ion beam (FIB), where the sharp interface clearly reveals the high-quality fabrication of the heterostructure. The flatness at the atomic scale suggests a low defect density on material surfaces. The vdW heterostructure composition is further demonstrated by the homogenous elemental distribution shown in energy-dispersive spectrometry (EDS) in the right panel of Figure 1d.

2.2. Nonvolatile Electronic/Optoelectronic Memory Triggered By Intense Electrical/Optical Stimuli

To comprehensively evaluate the nonvolatile electronic memory performance of the MoS_2/h-BN/Te heterostructure-based FG memory device, we characterized the memory window, switching speed, and retention stability. **Figure 2a** shows the transfer

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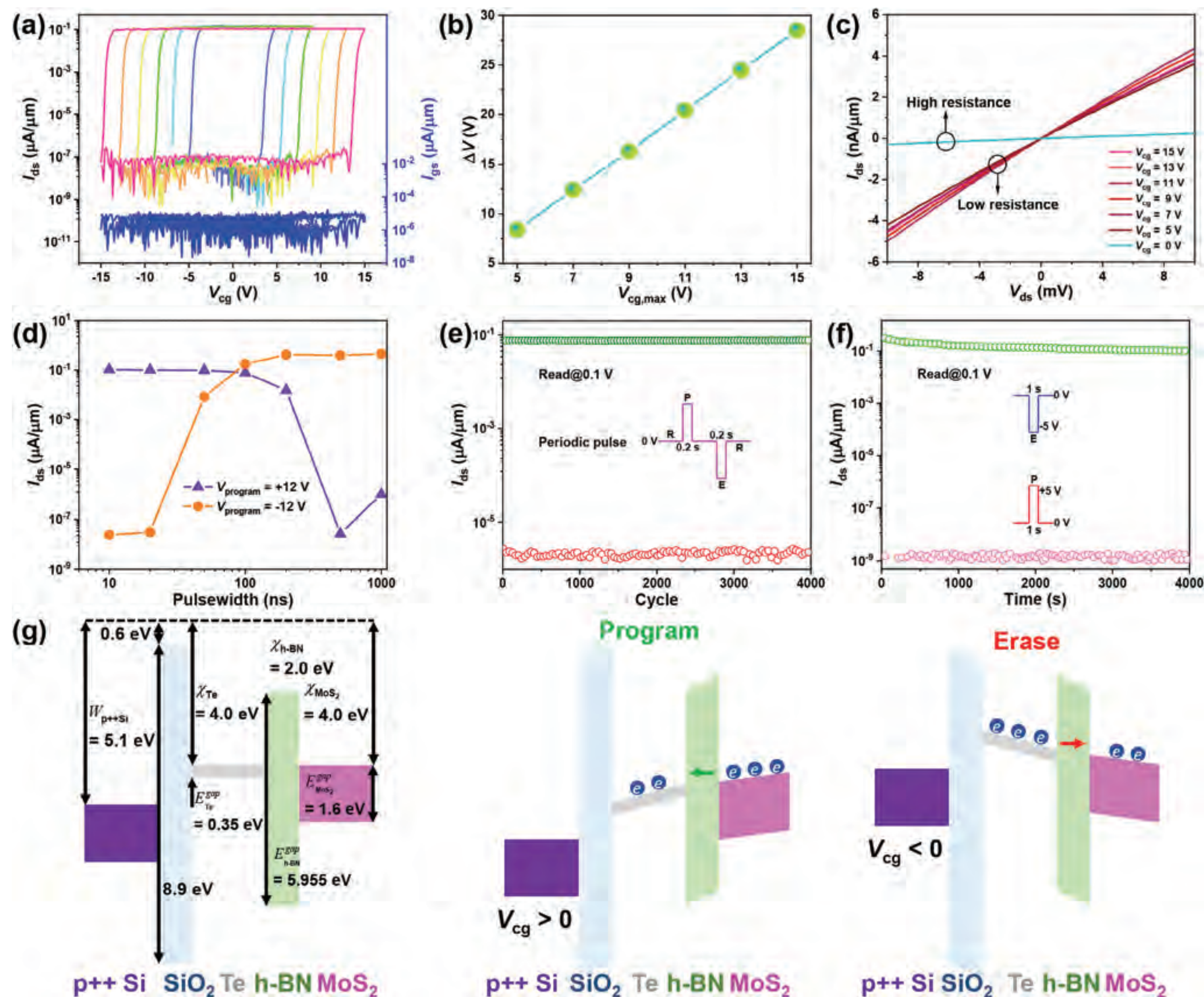

Figure 2. Nonvolatile electronic memory. a) Transfer curves with varying $V_{cg,max}$ from 5 to 15 V. V_{ds} = 0.1 V. The magnitude of the corresponding gate leakage currents is indicated by the right y-axis. b) Extracted memory window ΔV as a function of $V_{cg,max}$. c) Output curves characterized in a small electrical bias under different control gate voltages. d) Switching speed test of the FG memory device. The program and erase voltages are +12 and −12 V, respectively. V_{ds} = 0.1 V. e) Cycling endurance of the FG memory device. The applied program/erase voltages are ±10 V/0.2 s. f) Retention stability of the FG memory device. The high-/low-resistance states are switched by ±5 V/1 s electrical pulses. g) Energy band diagram of the FG memory device in different electronic memory states.

curves under different gate voltages. The threshold voltages vary significantly in the forward and backward sweeping directions, which fully demonstrate the charge trapping ability of the Te FG. To reduce the effect of contact resistance, we extracted the memory window from the transfer curves presented in Figure 2b using the Y-function method.[35,36] Note S1 (Supporting Information) details the extraction process of V_T. As shown in Figure S3 (Supporting Information), the extracted threshold voltage values are $V_T^{Forward}/V_T^{Backward}$ = −14.33/14.19 V when sweeping the control gate voltage from −15 to +15 V/+15 to −15 V, respectively. The memory window, defined as $\Delta V = V_T^{Backward} - V_T^{Forward}$ = 28.52 V corresponds to a ratio of 95.1% between the memory window range (W.R.) and the sweeping range (S.R.). More threshold voltage values, memory windows, and M.R./S.R. ratios under different control gate voltages are summarized in Table S1 (Supporting Information). The trapped charge density in the Te FG at ΔV = 28.52 V can be estimated by $n = \Delta V \epsilon_{h\text{-}BN} \epsilon_0 / q d_{Oxide} = 1.185 \times 10^{13} cm^{-2}$, where $\epsilon_{h\text{-}BN}$, ϵ_0, q, and d_{Oxide} are the relative permittivity of h-BN, permittivity of vacuum, elementary charge, and thickness of SiO_2, respectively.[37] This value is about two orders of magnitude higher than that in multilayer graphene, which fully implies the superiority of Te as the FG in FG memory devices.[38,39] Also, the linearly increased memory window versus maximum control gate voltage as shown in Figure 2b, indicates the strong tuning ability of the applied control gate voltage on charge storing in the Te FG. The output characteristic curves under different control gate voltages measured at a small bias voltage (V_{ds} = ±10 mV)

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are given in Figure 2c. Due to the electric field strength of the control gate voltages being weakened by the stored charge in the Te FG, the channel current exhibits only two distinct states (i.e., high-/low-resistance states). Moreover, the linear *I*–(*V* curve suggests that a good contact has been achieved during fabrication. The atomically sharp and clean interfaces between the vdW materials in this FG memory unit enable the extremely fast operations. The ultrafast switching speed (≈100 ns) of the fabricated device is demonstrated in Figure 2d. The detailed characterization process is illustrated in Figure S4 (Supporting Information). In the measurement, the electrical pulse amplitude for both programming/erasing (P/E) was kept at 12 V. In the programming process, electrical pulses with different pulse widths increasing from 10 ns to 1 µs were applied to control gate to switch the device (Figure S4a, Supporting Information). Based on the results, it can be concluded that the +12 V/100 ns pulse can slightly induce electron tunneling into the Te FG, while the +12 V/500 ns pulse can completely switch the device from a low-resistance state to a high-resistance state. In the erasing process, the −12 V/50 ns pulse is sufficient to "erase" the electrons stored in Te (Figure S4b, Supporting Information). The asymmetric switching speed in the programming/erasing processes is attributed to the different band movement under positive/negative external electric fields. In this study, applying a +12 V control gate pulse induced a downward movement for both Te and MoS_2 energy bands relative to h-BN, resulting in a higher effective tunneling barrier. Conversely, a −12 V electrical pulse induced an upward movement for both Te and MoS_2 energy bands, leading to a lower effective tunneling barrier. The lower effective tunneling barrier for electrons resulted in a faster erasing operation. The ultrafast programming/erasing electrical pulses with different pulse (widths ranging from 10 ns–1 µs) were generated by the B1500A semiconductor parameter analyzer and pulse waveforms were characterized by a digital oscilloscope (Tektronix TBS 1102B-EDU), as shown in Figure S5 (Supporting Information). To better evaluate the charge trapping ability in Te FG, we measured the direct threshold voltage after erasing and programing operations in near-zero control gate sweep, which is shown in Figure S6 (Supporting Information). We first applied a −10 V/1 s electrical pulse to erase the memory unit to the original state-1 and then applied a +10 V/1 µs electrical pulse to program the memory unit to state-0. We can observe that the threshold voltage shifts left over time and the state-0 in 4000 s is still clearly distinct from the original state-1, which fully demonstrates the considerable charge trapping ability of Te FG.

The FG device's cycling endurance is presented in Figure 2e, where it exhibits highly reproducible switching between low- and high-resistance states over 4000 cycles under periodic programming and erasing trains (P: +12 V/0.2 s, E: −12 V/0.2 s). The dynamic P/E behavior is illustrated in Figure S7 (Supporting Information). Two distinct states (high-resistance state (LRS) and low-resistance state (HRS)) retaining for over 4000 s presented in Figure 2f demonstrate the long-term memory stability of the FG device. Moreover, the high write and read margin (10^8) between LRS and HRS corroborates the considerable charge storage capacity of Te FG. On the other hand, after delicately controlling the charge quantity tunneling through h-BN dielectric by carefully tunning the electrical pulse width and amplitude at each time,[40,41] our device can also store multibit information within the write and read margin, which is shown in Figure S8 (Supporting Information), where 150 distinct potentiation/depression states are programmed by negative/positive electrical pulse trains (±5 V/1 µs), respectively.

The working mechanism of the device under electrical operation is illustrated in Figure 2g. The left panel depicts the energy band diagrams of different materials before being brought into contact, which is also supported by the Kelvin probe microscopy (KPFM) results (Figure S9, Supporting Information).[22,42–48] Figure S9a (Supporting Information) provides the optical microscopy image of a typical device for KPFM measurement, which is composed of MoS_2, h-BN, Te nanoflakes with similar thicknesses used in other devices. Figure S9c (Supporting Information) depicts the surface potential profile obtained along the light blue line in KPFM mapping of the overlapped area (Figure S9b, Supporting Information) and from which, we can conclude that the potential different between multilayer MoS_2 and Te nanoflake is very small. The band diagram of the device under programming operation is provided by the middle panel, where electrons in the MoS_2 channel will tunnel through the h-BN dielectric and be stored in the Te FG under the positive electrical pulse applied to the control gate. The resulting positive electric field will lead to the off-state in MoS_2. The right panel describes the erasing operation, where the stored electrons will tunnel back to the MoS_2 driven by the negative electrical pulse and recover the channel to the on-state.

The Fowler–Nordheim (F–N) plot was conducted to further evaluate the tunneling barrier for electrons at the h-BN/Te interface, and the results are shown in Figure S10 (Supporting Information). The stacked h-BN/Te heterostructure used for the F–N measurement is depicted in Figure S10a (Supporting Information), with the tunneling area (S = 93.75 µm^2) indicated by the purple dashed line. Figure S10b,c (Supporting Information) illustrates the measurement set-up and the band diagrams for direct/F–N tunneling, respectively. The temperature-independent *I*–*V* curve in Figure S10d (Supporting Information) demonstrates the quantum tunneling across the h-BN dielectric. Figure S10e (Supporting Information) shows the tunneling current (j_T) measured under forward bias at room temperature in logarithm scale. By replotting it as a F–N plot, i.e., $\ln (j_T/E^2_{h-BN})$ versus $1/E_{h-BN}$, the barrier height can be determined by the intercept (Figure S10f and its inset, Supporting Information). The value extracted by the F–N plot ($\Phi_{barrier}$ = 2.79 eV) is close to that (≈2 eV) given by Anderson's rule (Note S2 for more details, Supporting Information). The control gate voltage at which the F–N tunneling begins can be estimated by $V_{cg} = V_{FN}(d_{oxide} + d_{h-BN}/d_{h-BN}) \approx 10$ V, assuming similar dielectric constants for h-BN and SiO_2. It can be concluded that direct tunneling and F–N tunneling dominate at $V_{cg} < 10$ V and $V_{cg} > 10$V, respectively.

To further elucidate the electronic memory operations in the FG memory unit, we established an ideal physical model based on the equivalent circuit diagram (Figure S11, Supporting Information), please refer to Note S3 (Supporting Information) for detailed discussion.[10] This model indicates that the electric intensity in h-BN dielectric when using 50 nm SiO_2 dielectric is around 2 times of that when using 300 nm SiO_2 dielectric, that helps explain why the amplitude of control gate voltage (12 V) for ultrafast operations used in this work is much smaller than other

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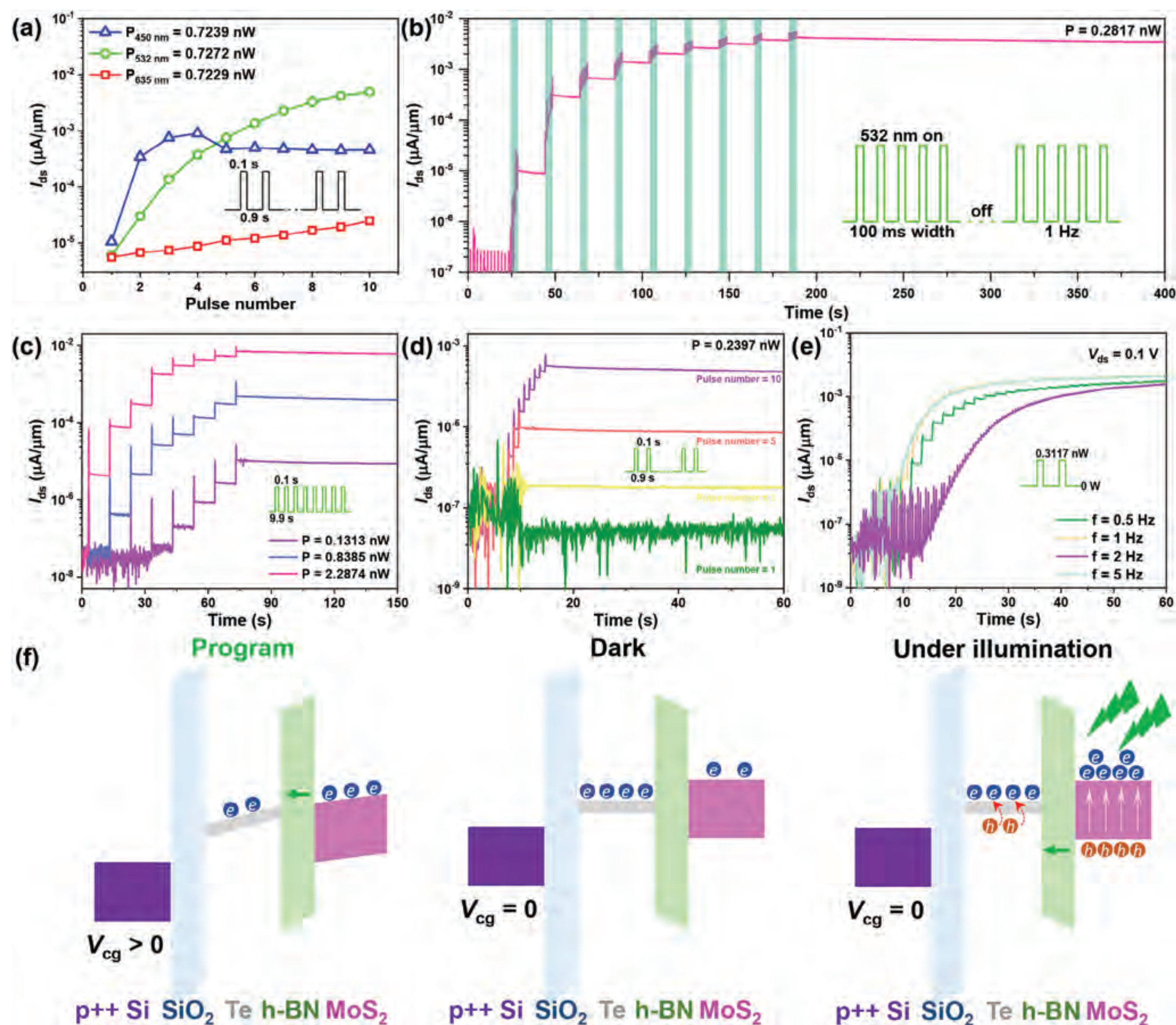

Figure 3. Nonvolatile optoelectronic memory. a) Photocurrent evolution triggered by optical pulse trains with different wavelength (blue: 450 nm, green: 532 nm, red: 635 nm). The laser power is kept as ≈0.72 nW. b) Nonvolatile optoelectronic memory tuned by illuminating laser pulse trains on the FG memory device. Each pulse train consists of five laser pulses. Photocurrent evolution tuned by laser pulse trains with c) different laser powers, d) different pulse numbers, and e) different frequencies (duty ratio = 90%). The read bias is kept as 0.1 V in all the measurements. f) Energy band diagram of the FG memory device in different optoelectronic memory states.

reports (≈20–30 V).[10,11] Moreover, this physical model can also be used to predict the ideal operation time in our FG memory device, which is shown in Figure S12 (Supporting Information). In erasing process, the ideal operation time is ≈8.5 ns under the control gate voltage of −12 V; in programming process, the ideal operation time is ≈17.2 ns under the control gate voltage of +12 V. These results suggest that the FG memory device performance can be further improved by optimizing the fabrication process.

This device exhibits nonvolatile multibit optoelectronic memory, as demonstrated in Figure 3; and Figures S13 and S14 (Supporting Information). Initially, red (635 nm), green (532 nm), and blue (450 nm) lights have been used to characterize the optoelectronic memory, and the results are presented in Figure 3a. The findings indicate that the FG device, based on the vdW MoS_2/h-BN/Te heterostructure, has an optimal photoresponse to green light at the same laser power level (≈0.72 nW); leading to the selection of 532 nm laser as the light source in subsequent measurements unless otherwise stated. Figure 3b illustrates the dynamic light-erase conductance evolution under periodic exposure to green laser pulses, with the laser pulse width, frequency, and power set to 100 ms, 1 Hz, and 0.2817 nW, respectively. Prior to each optical erasing, the MoS_2 channel was programmed using an electrical pulse to the high-resistance state. Subsequently, the MoS_2 conductance increases with increasing the number of optical pulse trains (each train includes 5 laser pulses) until saturation.

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Moreover, the multibit nonvolatile memory can be tuned by adjusting laser parameters. Figure 3c demonstrates the realization of 3-bit optical memory under various laser powers, where the laser pulse width and interval are 0.1 and 9.9 s, respectively. The dynamic multistate optical memory is presented in Figure 3d, where the channel current exhibits different resistance states by controlling the laser pulse numbers. The laser power is fixed at 0.2397 nW, the pulse frequency is 1 Hz, and the pulse width is 0.1 s. Varying the laser frequency also leads to an increase in the channel current with continuous exposure to laser pulses, as shown in Figure 3e. Figure S13 (Supporting Information) depicts the multilevel optical memory states, where more than 60 states are clearly distinguished. The long-term optical memory retention is demonstrated in Figure S14 (Supporting Information), where Figure S14a–d (Supporting Information) presents the channel current evolution triggered by different amounts of laser pulses. The insets provide the stepwise current evolution in the optical erasing processes. For comparison, the current evolution in the dark is given in Figure S14e (Supporting Information). As summarized in Figure S14f (Supporting Information), the multibit optical memory states with a large read margin of over 10^5 can maintain for over 1000 s. In the optical erasing process, the applied laser frequency, pulse width, and power are 1 Hz, 100 ms, and 0.3220 nW, respectively.

The working mechanism of the optoelectronic memory is illustrated in Figure 3f. Prior to each optical erasing operation, the FG device is programmed to a high-resistance state using a proper electrical pulse; left and middle panels illustrate the energy band diagram. Under illumination, photogenerated electron/hole pairs will accumulate in the MoS_2 channel. Part of the holes hold a certain probability to tunnel through the h-BN dielectric and neutralize the stored electrons in Te FG. This diminishes the effective electric field, as depicted in the right panel.

To highlight the advantages of using Te as the charge trapping layer in 2D FG devices, we compared the nonvolatile electronic/optoelectronic performance of our device with other reports, and the results are presented in **Table 1**. Our FG memory unit exhibits comparable electronic programming/erasing capabilities to those of the most advanced devices reported in the literature. Furthermore, its impressive optoelectronic memory behavior suggests potential applications in future in-sensor memory computing systems.

Moreover, Te can be utilized as an internal gate to enable a MoS_2 transistor, as demonstrated by the basic electrical characterization presented in Figure S15 (Supporting Information). Figure S15a (Supporting Information) illustrates the schematic of the MoS_2 transistor with the h-BN nanoflake serving as the gate dielectric. The linear output curves under small bias in Figure S15b (Supporting Information) indicate good contact between the source/drain electrodes and the channel material. The negligible hysteresis window displayed in Figure S15c (Supporting Information) confirms the clean interface between the MoS_2 and h-BN nanoflakes, consistent with the cross-section TEM results. The subthreshold swing (*SS*) values were further extracted from its transfer curves and the values are 69.08 and 64.95 mV dec^{-1} in forward and backward sweeping directions, respectively (Figure S15d, Supporting Information). These values are very close to the ideal limitation at room temperature (60 mV dec^{-1}) and help illustrate the good performance of Te FET.

2.3. Volatile Electronic/Optoelectronic Memory Triggered by Mild Electrical/Optical Stimuli

Charge trapping states are quite common in MoS_2 nanoflakes obtained by mechanical exfoliation, and they will bring up the current relaxation under mild electrical/optical stimuli thus laying the foundation for the MoS_2-based synaptic devices.[49,50] Here we also demonstrate that the volatile electronic/optoelectronic memory behaviors could be achieved in our multifunctional FG memory unit with using Te as the FG.

The volatile optoelectronic memory is illustrated in **Figure 4a–f**; and Figure S16 (Supporting Information). Figure 4a,b compares the optoelectronic current evolution triggered by laser pulses of different intensities. When an intense laser pulse is applied, the channel current reaches a higher value and then stabilizes. In contrast, when a weak optical pulse is used, the photocurrent quickly recovers to its initial state. Figure S16 (Supporting Information) shows the short-term memory states triggered by an optical pulse train with mild intensity. The laser power, pulse width, and interval are 0.1340 nW, 0.1 s, and 0.9 s, respectively. Figure 4c depicts the volatile optoelectronic memory behaviors triggered by optical pulse trains with varying pulse numbers. As the pulse numbers increase, both the peak value of the excitatory postsynaptic current (EPSC) and the recovery time will also increase. Figure 4d presents the EPSC triggered by optical pulse trains with different pulse intervals, demonstrating that the EPSC can be adjusted by controlling the stimulation parameters. The paired-pulse facilitation (PPF) effect triggered by optical stimulation is illustrated in Figure 4e and the optoelectronic PPF ratio $\Delta A_2/\Delta A_1 \times 100\%$ is provided as a function of the optical pulse interval is provided in Figure 4f. The PPF behavior triggered by paired optical pulses with different intervals is shown in Figure S17 (Supporting Information), from the bottom up, the interval increases from 1 to 10 s. The results are fit to a double exponential decay function: $PPF = C_0 + C_1 e^{-\Delta t/\tau_1} + C_2 e^{-\Delta t/\tau_2}$, indicated by the blue line in Figure 4f, where $\tau_1 = 2.4554$ s and $\tau_2 = 2.4560$ s, respectively.

After weakening the electrical stimuli intensity, our FG device also exhibits volatile electronic memory behavior. In Figure S18 (Supporting Information), we present the short-term memory state triggered by an electrical pulse with a mild intensity of −2 V and a pulse width of 100 ms. In contrast to the nonvolatile memory behavior triggered by intense electrical pulses, the EPSC in this case recovers to its initial state within several seconds. In Figure 4g, we illustrate the PPF behavior triggered by paired electrical pulses with different intervals, ranging from 0.1 to 1 s from the bottom up. The pulse amplitude and width are −2 V and 10 ms, respectively. Figure 4h provides an example of the PPF effect triggered by paired electrical pulse with an interval of 0.2 s. We define the electronic PPF ratio as $\Delta A_2/\Delta A_1 \times 100\%$ and present it as a function of the electrical pulse interval in Figure 4i. The results can be fitted by the double exponential decay function: $PPF = C_0 + C_1 e^{-\Delta t/\tau_1} + C_2 e^{-\Delta t/\tau_2}$, where $\tau_1 = 0.0672$ s and $\tau_2 = 0.3274$ s, respectively.

In addition, we also fabricated a device by carefully eliminating overlapping between the source/drain electrodes and Te nanoflake as the control experiment and this device exhibit similar memory behaviors obtained on the device throughout the

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Table 1. Comparison between different nonvolatile electronic/optoelectronic 2D FG devices.

Device structure	M.R./S.R./$V_{cg,max}$	Electronic Extinction Ratio	Electronic Switching Speed	Electronic Cycle Endurability	Electronic Retention	Optoelectronic Extinction Ratio	Optoelectronic Retention	Optoelectronic Multilevel	References
ReS_2/h-BN/graphene	83.3%/60 V	10^8	1 µs	>400	>4000 s	N.A.[a]	N.A.	N.A.	[53]
InSe/h-BN/graphene	80.0%/40 V	10^{10}	21 ns	>2000	>5400 s	N.A.	N.A.	N.A.	[10]
MoS_2/h-BN/graphene	75.7%/35 V	10^6	20 ns	>1390	>5300 s	N.A.	N.A.	N.A.	[11]
MoS_2/h-BN/graphene	N.A.	N.A.	N.A.	N.A.	N.A.	10^6	>30 000 s	18	[54]
PtS_2/h-BN/graphene	62.5%/40 V	10^7	N.A.	>1000	>1000 s	N.A.	N.A.	74	[55]
Graphene/h-BN/MoS_2	64.3%70 V	10^6	N.A.	N.A.	>10 000 s	10^6	>10 000 s	13	[56]
ReS_2/h-BN/MoS_2	80.0%/50 V	10^7	N.A.	>2000	>10 000 s	N.A.	>800 s	3	[19]
SnS_2/h-BN/graphene	81.0%/40 V	10^6	N.A.	>600	>4000 s	10^4	N.A.	>50	[17]
MoS_2/h-BN/Te	95.1%/15 V	10^8	P/E:[b] 500 ns/100 ns	>4000	>4000 s	>10^5	>1000 s	>60	This work

[a] **N.A.**: Not applicable; [b] **P/E**: Programming/Erasing.

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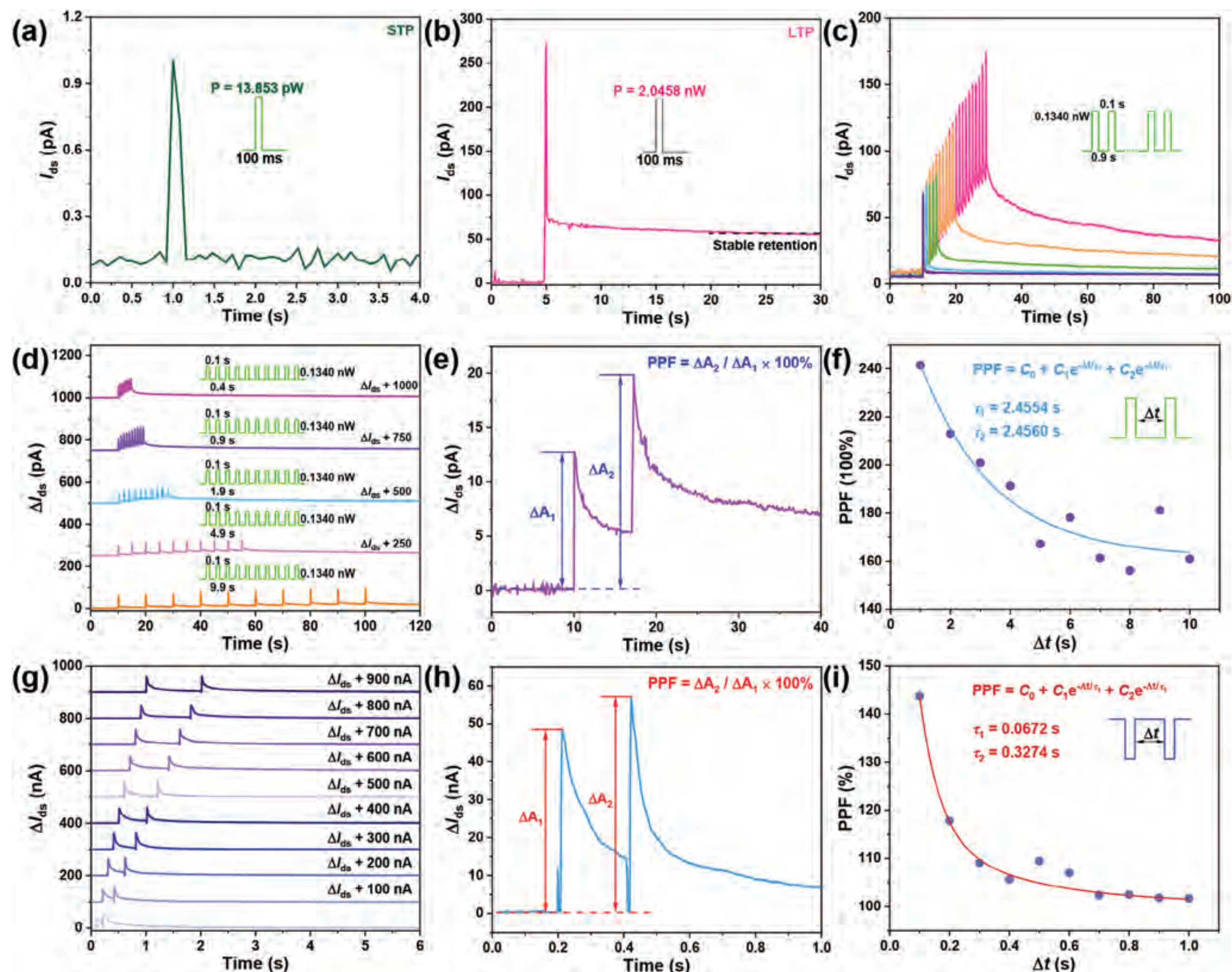

Figure 4. Volatile electronic/optoelectronic memory. a) Volatile optoelectronic memory behavior triggered by a weak optical pulse. b) Nonvolatile optoelectronic memory behavior triggered by an intense optical pulse. c) Volatile optoelectronic memory behavior stimulated by pulse trains with different pulse numbers. d) Volatile optoelectronic memory behavior stimulated by pulse trains with different pulse intervals. e) PPF effect induced by paired optical pulse. f) Optoelectronic PPF ratio defined as $\Delta A_2/\Delta A_1 \times 100\%$ as the function of the optical pulse interval. g) Current evolution triggered by paired electrical pulse with different intervals. h) PPF effect induced by paired electrical pulse. i) Electronic PPF ratio defined as $\Delta A_2/\Delta A_1 \times 100\%$ as the function of the electrical pulse interval.

manuscript (Figure S19, Supporting Information). This helps confirm the origin of the multifunctional memory behaviors is the used vdW materials and the effect of the metal electrode is trivial.

2.4. Multimodal Reservoir Computing

We leveraged the nonlinear dynamics of the FG device to stimulate a multimodal RC system. The Te FG device serves as the memory unit for classifying the N-MNIST database (Neuromorphic-Modified National Institute of Standards and Technology database). **Figure 5a** depicts the electronic/optoelectronic FG device used for electrical/optical signal sensing and processing. Using this device, we designed a RC system capable of directly learning and inferring from electrical/optical signals without additional dedicated transducers. RC systems typically comprise of three components: the input layer, the intermediate representation or reservoir, and the output layer. Only the weights of the output layer require training, reducing the training burden compared to traditional compared to traditional artificial neural networks (ANNs).[51,52] However, the challenge of processing multimodal signals with RC system lies in feature extraction and multisensory fusion. In conventional RC systems, multiple reservoirs are required for feature extraction because each reservoir can only respond to one type of input signal. These extracted features for different modalities are then integrated and classified by the readout layer, as shown in Figure 5b. In contrast, our electronic/optoelectronic FG device demonstrates an effective response to electrical/optical signals simultaneously, allowing for a mixed-input RC system that achieves both feature extraction and multisensory fusion within

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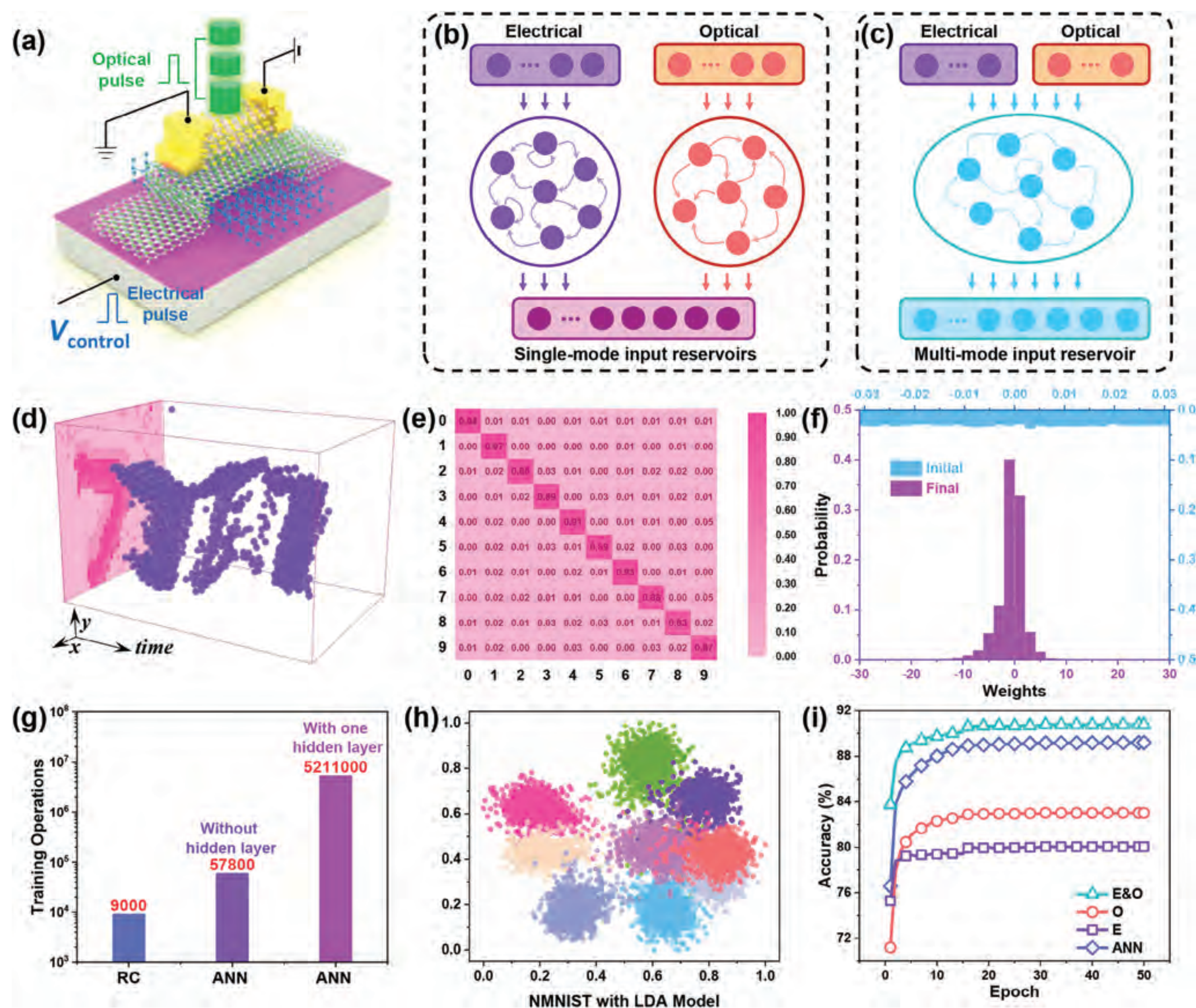

Figure 5. Multimodal RC computing. a) Schematic illustration of the optoelectronic FG memory unit and experimental set-up. b) Schematic illustration of the single-mode RC architecture. c) Schematic illustration of the multimodal RC architecture. d) A sample from the N-MNIST dataset. e) Confusion matrix on classifying the N-MNIST test set. f) Initial/final conductance distributions before/after training. g) Number of weights need to be trained for RC, ANN without hidden layer and with one hidden layer. h) Imensionality reduction of optoelectronic reservoir outputs using linear discriminative analysis (LDA). i) Recognition accuracy of the N-MNIST-based digit-recognition task for reservoirs working at different modes and software baseline (ANN).

a single reservoir (Figure 5c). Reducing the need for features extractions and multisensory fusion will greatly benefit the energy and time consumption, representing a significant advancement in the multimodal RC method over traditional RC systems.

The multimodal signal processing capability of our multimodal RC system enables it to be applied in long-distance communication technology, such as augmented reality and surveillance. It is well known the transmission speeds for sound signal and image signal usually vary a lot, in that case, the sound and image information encoded into electrical and optical spikes, respectively, need to be processed asynchronously. Besides processing synchronous electrical and optical signal in long-distance communication, our multimodal RC system will also find their applications in brain science, where the multimodal signal encoding is a must. To evaluate its performance in such scenarios, our multimodal RC system is applied to conduct the task of digit-recognition based on the N-MNIST dataset. The N-MNIST dataset was captured using a dynamic vision sensor (DVS) that was mounted on a motorized pan-tilt unit, which performed a saccade movement to capture images from frame-based static image datasets (MNIST). A sample from the N-MNIST dataset can be seen in Figure 5d. The event stream of the N-MNIST dataset has a slightly higher spatial resolution of 34 × 34 pixels compared to that of the MNIST dataset. Each recording was converted into 5 frames, and only the positive channel was used for every input. This frameless dataset contains additional temporal information while retaining similar spatial information to the original dataset. For this task,

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we assume that the upper half of the digits can only be sensed as electrical signals, and the lower half can only be sensed as visual signals, represented by optical and electrical pulses, respectively. The intensity of each pixel of an input frame denotes whether there is an electrical or optical pulse applied to the corresponding FG reservoir device in the sensor array. The possible inputs to one FG reservoir device across the 5 temporal frames form 5-bit vectors, corresponding to 32 illumination patterns (Figures S20–23, Supporting Information). The stability and repeatability of single device is demonstrated in Figure S24 (Supporting Information). We have sampled the response to each pattern (5-bit electrical pulse patterns and 5-bit optical pulse patterns) in the single device for several times and the mean/median and quartiles are visualized in a grouped box chart. The small current variations reveal the high stability of our device and its application potential in real multimodal RC system. The final currents of the FG reservoir devices in the array after receiving the five frames were used to perform pattern recognition through the trained software readout layer (Figure S25, Supporting Information).

The research findings reveal that when stimulated by single-modal electrical or optical pulses, only half of the digit was fed to the reservoir, resulting in unsatisfactory accuracies of 80.04% and 83.01%, respectively, as depicted in Figure 5i. However, a mixed-input fed to the reservoir produced a high recognition accuracy of 90.77% (indicated by the green dot in Figure 5i), even surpassing the software baseline (89.19%, indicated by the blue dot in Figure 5i). Figure 5e illustrates the confusion matrix in classifying the N-MNIST test set with mixed input, while Figure 5f presents the initial and final weights distribution in the readout layer, the latter shows a quasinormal distribution. Furthermore, Figure 5h demonstrates the 2D distribution of the extracted feature vectors produced by the multimodal reservoir using linear discriminant analysis (LDA) for dimensionality reduction. These encoded features have been effectively clustered in the 2D feature space, indicating the success of the nonlinear transformations by the volatile electronic/optoelectronic memory behavior triggered by weak stimuli in our device.

Finally, a comparison between RC and conventional ANNs for the N-MNIST-based digit-recognition task is made in terms of training cost, as shown in Figure 5g. The results demonstrate that a conventional two-layer fully connected neural network with 900 hidden units (same as the number of reservoir nodes) requires a significant number of weights to be trained (521 1000), which grows quickly with the network going deeper. However, this number remains constant (9000) for RC, further confirming the advantage of RC for real-time edge learning.

To further demonstrate the superiority of our multimodal RC system, we compared the classification accuracies achieved by using different methods (mixed optical and electrical input for the full and half digit dataset, single electrical input for the full and half digit dataset, and single optical input for the full and half digit dataset), which is shown in Figure S26 (Supporting Information). It can be found that the classification accuracy with mixed electrical and optical input for the full digit dataset is higher than single electrical or optical input for the full digit dataset and that also helps demonstrate the superiority of our multimodal RC system.

3. Conclusions

In summary, we have fabricated a 2D electronic/optoelectronic FG memory device with Te as the charge-trapping layer for multimodal RC. Thanks to the superior charge trapping ability of Te, this device exhibited excellent nonvolatile electronic memory behavior when stimulated by intense electrical/optical pulses, including a high extinction ratio ($\approx 10^8$), a close to unit (95.1%) ratio between the memory window range and sweeping range, a fast switching speed (≈100 ns), a long cycle (>4000 cycles), and retention (>4000 s) stability, or the long-term optoelectronic memory behavior (>1000 s) and nonvolatile multibit (>60) optoelectronic programmable characteristics. These performances are comparable to the most advanced 2D electronic/optoelectronic FG devices. We also demonstrated that the device's memory could degrade into volatile memory after weakening the input stimuli due to the charge trapping in MoS_2 channel. everaging the device's rich dynamics, we simulated a multimodal RC network that achieved a high recognition accuracy of 90.77% in the event-based N-MNIST digit-recognition task, parallel to that of the software baseline. This work offers new possibilities for advanced electronics/optoelectronics in the 2D family and provides design insights for future smart signal processing systems at the edge.

4. Experimental Section

Heterostructure Preparation and Device Fabrication: Te nanoflakes were synthesized using a hydrothermal method and deposited onto a SiO_2/Si substrate via drop-casting.[22,23] The Si substrate covered by 50 nm thermal oxide (SiO_2) was purchased from Silicon Valley Microelectronics, Inc., where the Si was heavily doped by boron in *p*-type and its resistivity is less than 0.005 ohm cm. The h-BN and MoS_2 nanoflakes were mechanically exfoliated on the polydimethylsiloxane (PDMS) directly from their maternal crystals, which were purchased from 2D Semiconductor Inc., and then transferred step-by-step onto the bottom heterostructure using a dry transfer method.[32] The electrodes were defined using a standard electron beam lithography (EBL) process (TESCAN, VEGA3), followed by the thermal evaporation of Cr/Au (8/60 nm).

Device Characterizations: The heterostructures were imaged using an optical microscope (Nikon, EBLIPSE LV100ND) and the false-color SEM image was processed using MOUNTAINS8 software based on the original SEM image captured from TESCAN, VEGA3. The height profiles of the vdW nanoflakes were characterized by AFM (Bruker, Dimension Icon with Scan Asyst), and the Raman spectra were obtained at room temperature using a Renishaw Raman Microscope with a polarized laser at a wavelength of 532 nm. Electronic memory behaviors were characterized using a B1500A semiconductor parameter analyzer, and the waveform of the electrical pulses was measured with a digital oscilloscope (Tektronix TBS 1102B-EDU). Optoelectronic memory behaviors were characterized on a custom-built platform under ambient conditions, where monochrome lasers (450, 532, and 635 nm) were combined with an optical chopper and guided to the device via an optical fiber. Channel current was monitored using an Agilent 4155C semiconductor analyzer (Agilent Technologies, Santa Clara, CA). In measuring the current evolution triggered by 5-bit electrical pulse trains, 32 (5-bit) electrical pulse trains ("00000" to "11 111," "0" represents the electrical pulse amplitude is zero and "1" represents the electrical pulse amplitude is nonzero) were generated by the B1500A semiconductor analyzer and the current evolution in MoS_2 channel was monitored by Agilent 4155C semiconductor analyzer; similarly, in characterizing the current evolution triggered by 5-bit optical pulse trains, 32 (5-bit) optical pulse trains ("00000" to "11 111," "0" represents the absence of a laser pulse to the device and "1" represents the presence of a laser pulse to the device) were generated by a monochrome laser (532 nm)

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modulated by a mechanical chopper. For each pulse train, after 5 consecutive laser pulses hit the device, then the light path was manually cut off.

Simulation of the Multimodal Reservoir Computing System with the FG Devices: The whole spike train in N-MNIST dataset can be represented as a $34 \times 34 \times 2 \times T_0$ sizedspike train, where "34" refers to the height and width of the sensing field, T_0 denotes the length of recording time, and "2" indicates that the DVS camera records the spike events in two channels—On and Off. In the experiments, the On channel was only used. To preprocess neuromorphic datasets, the event-to-frame integrating method was used and each recording was converted to 5 frames. The height and width of each sample were cropped from 34 to 30. The simulated multimodal RC system was created with 900 electrically/optically operated memory devices serving as the reservoir nodes. The conductance programming by both electrical and optical stimulus was calibrated using measurement data acquired on a single device. The readout layer consisted of a 900×10 fully connected network, with ten outputs representing ten different digits. The readout layer was implemented in software. The learning was performed by minimizing the categorical cross-entropy loss using mini-batch (batch size = 128) gradient descent with the Adam optimizer (initial learning rate = 0.01, step size = 15, gamma = 0.1), and the total training epoch was 50. All 60 000 event-based versions of the MNIST handwritten digits in the learning set were used in the learning stage and the 10 000 event-based digits of the test set were used for inference.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

2D van der Waals heterostructures, floating gate, multimodal reservoir computing, optoelectronic memory devices, tellurium nanoflake

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[1] Y. Liu, N. O. Weiss, X. Duan, H.-C. Cheng, Y. u Huang, X. Duan, *Nat. Rev. Mater.* **2016**, *1*, 16042.
[2] C. Tan, X. Cao, X.-J. Wu, Q. He, J. Yang, X. Zhang, J. Chen, W. Zhao, S. Han, G.-H. Nam, M. Sindoro, H. Zhang, *Chem. Rev.* **2017**, *117*, 6225.
[3] C. Liu, H. Chen, S. Wang, Q. Liu, Y.-G. Jiang, D. W. Zhang, M. Liu, P. Zhou, *Nat. Nanotechnol.* **2020**, *15*, 545.
[4] A. Sebastian, M. Le Gallo, R. Khaddam-Aljameh, E. Eleftheriou, *Nat. Nanotechnol.* **2020**, *15*, 529.
[5] S. Chen, M. R. Mahmoodi, Y. Shi, C. Mahata, B. Yuan, X. Liang, C. Wen, F. Hui, D. Akinwande, D. B. Strukov, M. Lanza, *Nat. Electron.* **2020**, *3*, 638.
[6] K. Liu, B. Dang, T. Zhang, Z. Yang, L. Bao, L. Xu, C. Cheng, R. Huang, Y. Yang, *Adv. Mater.* **2022**, *34*, 2108826.
[7] M. Farronato, P. Mannocci, M. Melegari, S. Ricci, C. Compagnoni, D. Ielmini, *Adv. Mater.* **2022**, *34*, 2205381.
[8] L. Sun, Z. Wang, J. Jiang, Y. Kim, B. Joo, S. Zheng, S. Lee, W. J. Yu, B.-S. Kong, H. Yang, *Sci. Adv.* **2021**, *7*, eabg1455.
[9] K. Liu, T. Zhang, B. Dang, L. Bao, L. Xu, C. Cheng, Z. Yang, R. Huang, Y. Yang, *Nat. Electron.* **2022**, *5*, 761.
[10] L. Wu, A. Wang, J. Shi, J. Yan, Z. Zhou, C. Bian, J. Ma, R. Ma, H. Liu, J. Chen, Y. Huang, W. Zhou, L. Bao, M. Ouyang, S. J. Pennycook, S. T. Pantelides, H.-J. Gao, *Nat. Nanotechnol.* **2021**, *16*, 882.
[11] L. Liu, C. Liu, L. Jiang, J. Li, Y. Ding, S. Wang, Y.-G. Jiang, Y.-B. Sun, J. Wang, S. Chen, D. W. Zhang, P. Zhou, *Nat. Nanotechnol.* **2021**, *16*, 874.
[12] X. Wang, C. Zhu, Y. Deng, R. Duan, J. Chen, Q. Zeng, J. Zhou, Q. Fu, L. You, S. Liu, J. H. Edgar, P. Yu, Z. Liu, *Nat. Commun.* **2021**, *12*, 1109.
[13] J. A. Carballo, W. T. J. Chan, P. A. Gargini, A. B. Kahng, S. Nath, in *2014 IEEE 32nd International Conference on Computer Design (ICCD)*, IEEE, Seoul, South Korea **2014**, p. 139.
[14] G. Migliato Marega, Y. Zhao, A. Avsar, Z. Wang, M. Tripathi, A. Radenovic, A. Kis, *Nature* **2020**, *587*, 72.
[15] X. Sun, C. Zhu, J. Yi, L.i Xiang, C. Ma, H. Liu, B. Zheng, Y. Liu, W. You, W. Zhang, D. Liang, Q. Shuai, X. Zhu, H. Duan, L. Liao, Y. Liu, D. Li, A. Pan, *Nat. Electron.* **2022**, *5*, 752.
[16] B. Mukherjee, A. Zulkefli, K. Watanabe, T. Taniguchi, Y. Wakayama, S. Nakaharai, *Adv. Funct. Mater.* **2020**, *30*, 2001688.
[17] F. Gao, X. Zhang, B. Tan, S. Zhang, J. Zhang, D. Jia, Y. Zhou, P. Hu, *Small* **2021**, *17*, 2104459.
[18] H. Lai, Y. Zhou, H. Zhou, N. Zhang, X. Ding, P. Liu, X. Wang, W. Xie, *Adv. Mater.* **2022**, *34*, 2110278.
[19] Y. Wang, E. Liu, A. Gao, T. Cao, M. Long, C. Pan, L. Zhang, J. Zeng, C. Wang, W. Hu, S.-J. Liang, F. Miao, *ACS Nano* **2018**, *12*, 9513.
[20] W. Wu, G. Qiu, Y. Wang, R. Wang, P. Ye, *Chem. Soc. Rev.* **2018**, *47*, 7203.
[21] Z. He, Y. Yang, J.-W. Liu, S.-H. Yu, *Chem. Soc. Rev.* **2017**, *46*, 2732.
[22] Y. Wang, G. Qiu, R. Wang, S. Huang, Q. Wang, Y. Liu, Y. Du, W. A. Goddard, M. J. Kim, X. Xu, P. D. Ye, W. Wu, *Nat. Electron.* **2018**, *1*, 228.
[23] M. Amani, C. Tan, G. Zhang, C. Zhao, J. Bullock, X. Song, H. Kim, V. R. Shrestha, Y. Gao, K. B. Crozier, M. Scott, A. Javey, *ACS Nano* **2018**, *12*, 7253.
[24] C. Zhao, C. Tan, D.-H. Lien, X. Song, M. Amani, M. Hettick, H. Y. Y. Nyein, Z. Yuan, L. Li, M. C. Scott, A. Javey, *Nat. Nanotechnol.* **2020**, *15*, 53.
[25] P. Yang, J. Zha, G. Gao, L. Zheng, H. Huang, Y. Xia, S. Xu, T. Xiong, Z. Zhang, Z. Yang, Y. Chen, D.-K. Ki, J. J. Liou, W. Liao, C. Tan, *Nano-Micro Lett.* **2022**, *14*, 109.
[26] J. Zha, S. Shi, A. Chaturvedi, H. Huang, P. Yang, Y. Yao, S. Li, Y. Xia, Z. Zhang, W. Wang, H. Wang, S. Wang, Z. Yuan, Z. Yang, Q. He, H. Tai, E. H. T. Teo, H. Yu, J. C. Ho, Z. Wang, H. Zhang, C. Tan, *Adv. Mater.* **2023**, *35*, 2211598.
[27] J. Chen, T. Zhang, J. Wang, L. Xu, Z. Lin, J. Liu, C. Wang, N. Zhang, S. P. Lau, W. Zhang, M. Chhowalla, Y. Chai, *Sci. Adv.* **2022**, *8*, eabn3837.
[28] J. Chen, Y. Zhou, J. Yan, J. Liu, L. Xu, J. Wang, T. Wan, Y. He, W. Zhang, Y. Chai, *Nat. Commun.* **2022**, *13*, 7758.

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[29] M. Hirayama, R. Okugawa, S. Ishibashi, S. Murakami, T. Miyake, *Phys. Rev. Lett.* **2015**, *114*, 206401.
[30] D.-Q. Yang, L.-Q. Zhu, J.-L. Wang, W. Xia, J.-Z. Zhang, K. Jiang, L.-Y. Shang, Y.-W. Li, Z.-G. Hu, *Phys. Status Solidi B* **2022**, *259*, 2100625.
[31] P. Bhaskar, A. W. Achtstein, M. J. W. Vermeulen, L. D. A. Siebbeles, *J. Phys. Chem. C* **2019**, *123*, 841.
[32] H.-W. Guo, Z. Hu, Z.-B. Liu, J.-G. Tian, *Adv. Funct. Mater.* **2021**, *31*, 2007810.
[33] R. Geick, C. H. Perry, G. Rupprecht, *Phys. Rev.* **1966**, *146*, 543.
[34] H. Li, Q. Zhang, C. C. R. Yap, B. K. Tay, T. H. T. Edwin, A. Olivier, D. Baillargeat, *Adv. Funct. Mater.* **2012**, *22*, 1385.
[35] D. Schroder, *Semiconductor Material and Device Characterization*, Vol. *101*, John Wiley & Sons. Inc., Publication, Canada **2006**.
[36] H.-Y. Chang, W. Zhu, D. Akinwande, *Appl. Phys. Lett.* **2014**, *104*, 113504.
[37] A. Laturia, M. L. Van De Put, W. G. Vandenberghe, *Npj 2D Mater. Appl.* **2018**, *2*, 6.
[38] D. Qiu, D. U. Lee, K. S. Lee, S. W. Pak, E. K. Kim, *Nano Res.* **2016**, *9*, 2319.
[39] W. Zhu, V. Perebeinos, M. Freitag, P. Avouris, *Phys. Rev. B* **2009**, *80*, 235402.
[40] Z.-C. Zhang, Y. Li, J. Li, X.-D. Chen, B.-W. Yao, M.-X. Yu, T.-B. Lu, J. Zhang, *Adv. Funct. Mater.* **2021**, *31*, 2102571.
[41] O. h. H. Gwon, J. Y. Kim, H. S. Kim, S.-J. Kang, H. R. Byun, M. Park, D. S. Lee, Y.-J. Kim, S. Ahn, J. Kim, S.-J. Cho, Y.-J. Yu, *Adv. Funct. Mater.* **2021**, *31*, 2105472.
[42] H. Wu, Y. Cui, J. Xu, Z. Yan, Z. Xie, Y. Hu, S. Zhu, *Nano Lett.* **2022**, *22*, 2328.
[43] Z. Lin, J. Wang, J. Chen, C. Wang, J. Liu, W. Zhang, Y. Chai, *Adv. Electron. Mater.* **2022**, *8*, 2200380.
[44] A. Coker, T. Lee, T. P. Das, *Phys. Rev. B* **1980**, *22*, 2968.
[45] G.-H. Lee, Y.-J. Yu, C. Lee, C. Dean, K. L. Shepard, P. Kim, J. Hone, *Appl. Phys. Lett.* **2011**, *99*, 243114.
[46] J. Wang, F. Ma, W. Liang, M. Sun, *Mater. Today Phys.* **2017**, *2*, 6.
[47] C. Liu, X. Yan, X. Song, S. Ding, D. W. Zhang, P. Zhou, *Nat. Nanotechnol.* **2018**, *13*, 404.
[48] E. Zhang, W. Wang, C. Zhang, Y. Jin, G. Zhu, Q. Sun, D. W. Zhang, P. Zhou, F. Xiu, *ACS Nano* **2015**, *9*, 612.
[49] M. Zhang, Z. Fan, X. Jiang, H. Zhu, L. Chen, Y. Xia, J. Yin, X. Liu, Q. Sun, D. W. Zhang, *Nanophotonics* **2020**, *9*, 2475.
[50] M. M. Islam, D. Dev, A. Krishnaprasad, L. Tetard, T. Roy, *Sci. Rep.* **2020**, *10*, 21870.
[51] Y. Zhong, J. Tang, X. Li, B. Gao, H. Qian, H. Wu, *Nat. Commun.* **2021**, *12*, 408.
[52] C. Du, F. Cai, M. A. Zidan, W. Ma, S. H. Lee, W. D. Lu, *Nat. Commun.* **2017**, *8*, 2204.
[53] E. Wu, Y. Xie, S. Wang, D. Zhang, X. Hu, J. Liu, *Nanoscale* **2020**, *12*, 18800.
[54] M. D. Tran, H. Kim, J. S. Kim, M. H. Doan, T. K. Chau, Q. A. Vu, J.-H. Kim, Y. H. Lee, *Adv. Mater.* **2019**, *31*, 1807075.
[55] Y. Chen, J. Yu, F. Zhuge, Y. He, Q. Zhang, S. Yu, K. Liu, L. Li, Y. Ma, T. Zhai, *Mater. Horiz.* **2020**, *7*, 1331.
[56] W. Huang, L. Yin, F. Wang, R. Cheng, Z. Wang, M. G. Sendeku, J. Wang, N. Li, Y. Yao, X. Yang, C. Shan, T. Yang, J. He, *Adv. Funct. Mater.* **2019**, *29*, 1902890.

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